Remarks

Claims 9-16 are pending in the application and are presented for reconsideration. Claims 1-8 and 17 are canceled. Claims 9 and 15 have been amended; and claims 10-14 remain in the application unchanged. No new matter has been added.

Claim Rejections

Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Olisar et al. (U.S. Pat. 4,873,456) in view of Japanese reference JP 5-37305.

The Examiner's rejections of the claims are respectfully traversed.

Response to Rejections of Claims Under 35 U.S.C. § 102

a. Claims 9-14

Claim 9 recites:

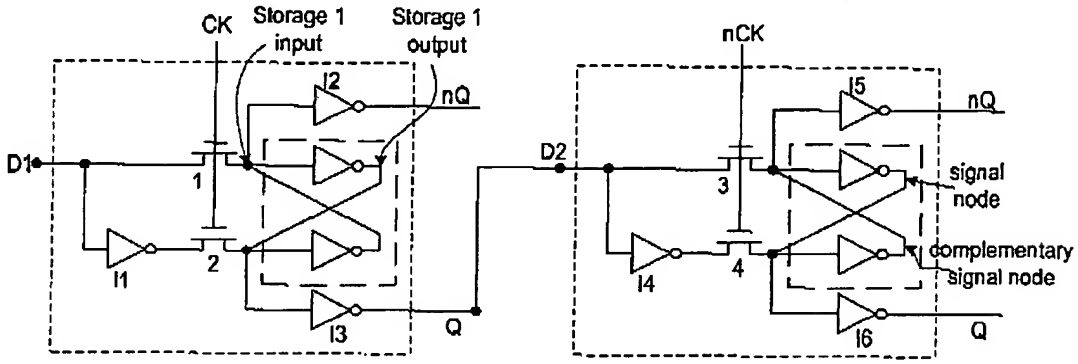
> A circuit, comprising:
> an input conveying an input signal;
> a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal;
> a first storage node having an input coupled to the first pass gate and having an output storing the first signal;
> a second pass gate connected to the output of the first storage node and enabling a second signal in response to the first signal stored on the output of the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal;
> a first inverter connected to the output of the first storage node and generating a first inverted signal in response to the first signal stored on the output of the first storage node;
> a third pass gate connected to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and
> an unclocked second storage node having a signal node coupled to the second pass gate and having a complementary signal node coupled to the third pass gate, the signal node storing the second signal and the complementary signal node storing the third signal.

The Examiner cites Figure 1 of Olisar et al. as showing a configuration of a master-slave flip-flops having two D flip-flop circuits connected in series,

wherein the master flip flop (12) and slave flip flop (14) are respectively clocked by a true and a complement clock signal.

The Applicant agrees with the Examiner that Olisar et al. does not show the detailed structure of each D flip flop. The Examiner cites JP 5-37305 as showing a detailed structure of a D flip flop. The Examiner included an illustration of the schematic diagram that would result by combining the D flip flops connected in series as shown in Figure 1 of Olisar with the detailed internal structure shown in Figure 1 of JP 5-37305. However, the Applicant respectfully disagrees with the Examiner's illustration of what the combination would look like.

The Applicant has supplied a schematic diagram below which details what the combination of Figure 1 of Olisar with the detailed internal structure shown in Figure 1 of JP 5-37305 would look like.



ILLUSTRATIVE SCHEMATIC

As noted in Olisar et al., the Q output of D flip flop 12 connects directly to the D input of D flip flop 14. Furthermore, the output of the circuit is taken at the Q output of the D flip flop 14.

In the Examiner's illustration, the Q output of the first flip flop is not connected to the D input of the second flip flop as would be the case if Olisar were to be combined with JP 5-37305. Instead, the Examiner connects the output of the first storage node to the D input of the second flip flop. However,

this is not what Olisar teaches, and one cannot read into a reference something that is not explicitly or implicitly there.

In addition, in JP 5-37305, the Q output is the non-inverted signal (having passed through inverter I1 and then inverter I3), and the nQ output is the inverted signal (having passed through only inverter I2). Thus, the output of inverter I3 should be connected to the D input of the second flip flop.

Noting the structure of the illustrative schematic contained herein, Olisar in combination with JP 5-37305 does not teach or suggest "a second pass gate connected to the output of the first storage node" as recited in Applicant's Claim 9. As shown in the illustrative schematic, the second pass gate (3) is not *connected* to the output of the first storage node. Rather, second pass gate (3) is connected to the output of inverter I3. Thus, Olisar in combination with JP 5-37305 does not meet this limitation.

Olisar in combination with JP 5-37305 also does not teach or suggest "a third pass gate connected to the first inverter" as recited in Applicant's Claim 9. As shown in the illustrative schematic, the third pass gate (4) is connected to the output of inverter I4. However, I4 is not "*connected* to the output of the first storage node" as recited in Applicant's Claim 9, and therefore I4 cannot be equated with Applicant's recited "first inverter". Thus, Olisar in combination with JP 5-37305 also does not meet this limitation.

Since Olisar in combination with JP 5-37305 does not teach an equivalent element for either the "second pass gate" or the "third pass gate", Olisar in combination with JP 5-37305 also does not teach "an unclocked second storage node having a signal node coupled to the *second pass gate* and having a complementary signal node coupled to the *third pass gate*".

Since Olisar in combination with JP 5-37305 does not teach an equivalent element for either the "second pass gate" or the "third pass gate", Olisar in combination with JP 5-37305 also does not teach "enabling a *second signal*" or "enabling a *third signal*", respectively.

Since Olisar in combination with JP 5-37305 does not teach an equivalent element for either "a second signal" or "a third signal", Olisar in combination with

JP 5-37305 also does not teach a "signal node storing the *second signal*" or a "complementary signal node storing the *third signal*".

Since Olisar in combination with JP 5-37305 does not meet each and every limitation of Applicant's claim 1, Olisar in combination with JP 5-37305 cannot be combined to formulate an obvious-type rejection under 35 U.S.C. § 103. Accordingly, Applicant respectfully submits that the rejection of claim 9 should be withdrawn and that claim 9 is now in position for allowance.

Claims 10-14 each depend from independent base claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 2-10 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 2-10 should be withdrawn.

b. Claims 15-16

Amended claim 15 recites:

> A method of operating a differential register, the differential register comprising a first pass gate having a first pass gate data input, a first pass gate enable input, and a first pass gate output; a first storage node having an input coupled to the first pass gate output and having an output; a second pass gate having a second pass gate data input connected to the output of the first storage node and the first pass gate output, a second pass gate enable input, and a second pass gate output; a first inverter having a first inverter input connected to the output of the first storage node and the first pass gate output and a first inverter output; a third pass gate having a third pass gate data input connected to the first inverter output, a third pass gate enable input, and a third pass gate output; an output node, and a complimentary output node, the method comprising the steps of:
>
> receiving a data input signal on the first pass gate data input and a master clock signal on the first pass gate enable input;
>
> conveying the data input signal from the first pass gate data input to the first pass gate data output and storing the data input signal on the output of the first storage node when the master clock signal is in a first master clock signal state;
>
> receiving the stored data input signal on the second pass gate input and a slave clock signal on the second pass gate enable input;
>
> conveying the stored data input signal from the second pass gate data input to the second pass gate data output for storage in the second storage node when the slave clock signal is in a first slave clock signal

state, wherein the slave clock signal is a compliment to the master clock signal;

inverting the stored input data signal to generate an inverted stored input data signal;

receiving the inverted stored data input signal on the third pass gate input and the slave clock signal on the third pass gate enable input;

conveying the inverted stored data input signal from the third pass gate data input to the third pass gate data output for storage in the second storage node when the slave clock signal is in the first slave clock signal state; and

on power-up, conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node regardless of states of the master clock signal and the slave clock signal.

Claim 15 recites limitations similar to Claim 1, including "a second pass gate having a second pass gate data input connected to the output of the first storage node" and "a third pass gate having a third pass gate data input connected to the first inverter output". For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claim 15 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 15 should be withdrawn.

Claim 16 depends from independent base claim 15 and add further limitations. For at least the same reasons that Claim 15 is not shown, taught, or disclosed by the cited references, Claim 16 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 16 should be withdrawn.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 9-16 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Jessica Costa

Jessica Costa, Reg. No. 41,065

The Law Offices of Jessica Costa, PC
P.O. Box 460 Crozet, VA
22932-0460
(434) 823-2232
(434) 823-2242 (fax)